CLAIMS

1. A semiconductor structure containing a field oxide, comprising:

a semiconductor substrate including an isolation region and an active region;

a field oxide formed on the semiconductor substrate in the isolation region;

a first pad layer formed on the semiconductor substrate in the active region;

a second pad layer formed on the semiconductor substrate not covered by the first pad layer, wherein the second pad layer has a smaller thickness than the first pad layer;

a mask layer formed on the first pad layer, wherein the mask layer has a larger width than the first pad layer to form a cavity beneath the mask layer and next to the first pad layer; and

a mask filler filled in the cavity.

2. The semiconductor structure as claimed in claim 1, wherein the first pad layer is an oxide.

3. The semiconductor structure as claimed in claim 1, wherein the second pad layer is an oxide.

4. The semiconductor structure as claimed in claim 1, wherein the first pad layer has a thickness of 100 Å to 250 Å.

5. The semiconductor structure as claimed in claim 1, wherein the second pad layer has a thickness of 60 Å to 120 Å.

6. The semiconductor structure as claimed in claim 1, wherein the mask layer is a nitride.

7. The semiconductor structure as claimed in claim 1, wherein the mask filler is a nitride.

8. The semiconductor structure as claimed in claim 1, wherein the cavity is indented from the sidewall of the mask layer by 300 Å to 700 Å.

9. A semiconductor structure containing a field oxide, comprising:

a semiconductor substrate including an isolation region and an active region;

a field oxide formed on the semiconductor substrate in the isolation region;

a first pad layer formed on the semiconductor substrate in the active region;

a second pad layer formed on the semiconductor substrate not covered by the first pad layer, wherein the second pad layer has a smaller thickness than the first pad layer;

a mask layer formed on the first pad layer, wherein the mask layer has a larger width than the first pad layer to form a cavity beneath the mask layer and next to the first pad layer; and

a mask liner formed on the sidewall of the mask layer and filled in the cavity, wherein the mask liner has a width of 0 Å to 50 Å from the sidewall of the mask layer.

10. The semiconductor structure as claimed in claim 9, wherein the mask liner is a nitride.

11. A method for fabricating a field oxide on a semiconductor substrate, comprising the steps of:

(a) successively forming a first pad oxide layer and a first mask layer;

(b) forming an opening in the first mask layer to define a region for forming the field oxide;

(c) removing the first pad layer exposed by the opening to form a cavity;

(d) forming a second pad layer having a smaller thickness than the first pad layer on the semiconductor substrate not covered by the first pad layer;

(e) conformably forming a second mask layer on the semiconductor substrate and the first mask layer to fill the mask portion into the cavity;

(f) isotropically etching the second mask layer to leave a mask filler in the cavity; and

(g) carrying out thermal oxidation to form the field oxide in the opening.

12. The method as claimed in claim 11, wherein step (c) is conducted by wet etching.

13. The method as claimed in claim 11, wherein step (d) is conducted by thermal oxidation.

14. The method as claimed in claim 11, wherein step (f) is conducted by isotropic RIE using plasma of a fluorine-containing gas as an etching reactive gas.

15. The method as claimed in claim 14, wherein step (f) is conducted by isotropic RIE using plasma of nitrogen fluoride (NF_3), SF_6, or CF_4 as an etching reactive gas.

16. The method as claimed in claim 15, wherein step (f) is conducted by isotropic RIE using plasma of SF_6 as an etching reactive gas.

17. A method for fabricating a field oxide on a semiconductor substrate, comprising the steps of:

(a) successively forming a first pad oxide layer and a first mask layer;

(b) forming an opening in the first mask layer to define a region for forming the field oxide;

(c) removing the first pad layer exposed by the opening to form a cavity;

(d) forming a second pad layer having a smaller thickness than the first pad layer on the semiconductor substrate not covered by the first pad layer;

(e) conformably forming a second mask layer on the semiconductor substrate and the first mask layer to fill the mask portion into the cavity;

(f) isotropically etching the second mask layer to leave a mask liner on the sidewall of the first mask layer and in the cavity, wherein the mask liner has a width of 0 Å to 50 Å from the sidewall of the first mask layer; and

(g) carrying out thermal oxidation to form the field oxide in the opening.